

## Partial Translation of D2 (JP H07-045948 A)

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Title: Multilayer Wiring Board and Process for Making Same

## Claim 1

A multilayer circuit board (6,7) comprising interlaminar insulating layers made of a resin ( $I_1, I_2, I_3, I_4$ ) and metal conductor patterns ( $C_2, C_3, C_4, C_5, C_6$ ), which interlaminar insulating layers and the metal conductor patterns are alternately laminated on a substrate board (1,4), wherein the metal conductor patterns ( $C_2 - C_6$ ) comprises a metal thin film layer ( $L_1$ ) formed by sputtering a metal capable of enhancing adhesion of the metal conductor patterns ( $C_2 - C_6$ ), and a copper plated layer ( $L_3$ ) formed on the metal thin film layer ( $L_1$ ).

## Claim 2

A multilayer circuit board (6,7) comprising interlaminar insulating layers made of a resin ( $I_1, I_2, I_3, I_4$ ) and metal conductor patterns ( $C_2, C_3, C_4, C_5, C_6$ ), which interlaminar insulating layers and the metal conductor patterns are alternately laminated on a substrate board (1,4), wherein the metal conductor patterns ( $C_2 - C_6$ ) comprises a metal thin film layer ( $L_1$ ) formed by sputtering a metal capable of enhancing adhesion of the metal conductor patterns ( $C_2 - C_6$ ), a copper thin film layer ( $L_2$ ) formed by sputtering copper on the metal thin film layer ( $L_1$ ), and a copper plated layer ( $L_3$ ) formed on the copper thin film layer ( $L_2$ ).

Page 4, paragraphs [0021], [0023]

A first conductor pattern composed of one or, if desired, more kinds of metal is formed on the above-mentioned substrate board by a conventional film forming procedure such as, for example, sputtering. ..(partially omitted)..

As specific examples of the resin constituting the

interlaminar insulating layers, there can be mentioned, for example, polyimide resin, polyamide resin, epoxy resin, BT(bismaleimide-triazine) resin, BCB (divinylsiloxanebisbenzocyclobutene) resin, polyester resin, modified polyimide resin, modified BT resin, modified epoxy resin, triazine resin, polybutadiene resin, polysulfone resin, polyether-polysulfone resin, polyetherimide resin, polyphenylene oxide resin, phenolic resin and urea resin.

Page 5, paragraphs [0028], [0029]

On the surface-treated first interlaminar insulating layer, a metal thin film layer composed of a metal capable of enhancing adhesion of a metal conductor pattern is formed. Further, on the metal thin film layer, a copper thin film layer is formed by sputtering copper. Thus, a primary layer composed of one or two kinds of metals is formed on the surface-treated first interlaminar insulating layer.

The metal capable of enhancing adhesion of a metal conductor pattern includes, for example, chromium, nickel, titanium, iron, tungsten, molybdenum, aluminum and cobalt. The metal thin film layer formed by sputtering such metal is densified and has smooth surface, and exhibits high adhesion to the interlaminar insulating layer.

# PATENT ABSTRACTS OF JAPAN

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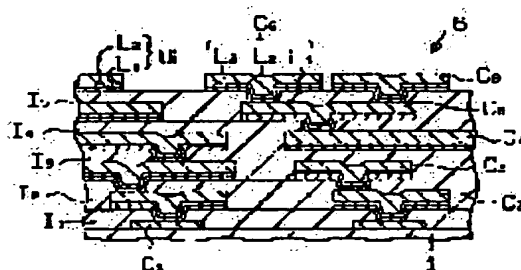
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## (54) MULTILAYER WIRING BOARD AND ITS MANUFACTURE

### (57)Abstract:

**PURPOSE:** To obtain a conductor pattern hard to strip even when an interlayer insulating layer is not roughened by chemicals by a method wherein the conductor pattern is constituted of a metal thin layer formed in such a way that a metal capable of enhancing the close contact property of the conductor pattern has been sputtered and of a copper-plated layer formed on the metal thin layer.

**CONSTITUTION:** Since a multilayer wiring board 6 uses a metal such as chromium or the like capable of enhancing the close contact property of conductor patterns C1 to C5 as a metal for formation of a metal thin film, it is possible to obtain the conductor patterns hard to strip. In addition, a metal thin layer L1 formed by a sputtering operation is generally dense and smooth, and its adhesion force is excellent. As a result, the metal thin layer TL is used as a substratum for a copper-plated layer L3, and the close contact property of the conductor patterns C1 to C5 can be enhanced even when interlayer insulating layers I1 to I5 are not roughened by chemicals.



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CLAIMS

[Claim(s)]

[Claim 1] In the multilayer-interconnection plate (6 7) which comes to carry out laminating formation of the layer insulation layer made of resin (11, 12, 13, 14, and 15), and the metal conductor pattern (C2, C3, C4, C5, and C6) on a substrate (1 4) by turns. The metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern (C2 - C6) (L1). The multilayer-interconnection plate equipped with the conductor pattern (C2 - C6) constituted by the copper-plating layer (L3) formed on said metal thin layer (L1).

[Claim 2] In the multilayer-interconnection plate (6 7) which comes to carry out laminating formation of the layer insulation layer made of resin (11, 12, 13, 14, and 15), and the metal conductor pattern (C2, C3, C4, C5, and C6) on a substrate (1 4) by turns. The metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern (C2 - C6) (L1). The multilayer-interconnection plate equipped with the conductor pattern (C2 - C6) constituted by the copper thin layer (L2) formed by carrying out sputtering of the copper on said metal thin layer (L1), and the copper-plating layer (L3) formed on said copper thin layer (L2).

[Claim 3] In the manufacture approach of the multilayer-interconnection plate (6 7) which carries out laminating formation of the layer insulation layer made of resin (11, 12, 13, 14, and 15), and the metal conductor pattern (C2, C3, C4, C5, and C6) by turns on a substrate (1 4) it is following (a) at least. - (e) The manufacture approach of the multilayer-interconnection plate characterized by performing a process one by one : (a) By carrying out the spin coat of the resin on a substrate (1 4) The process and (b) which form a layer insulation layer (11 -15) By performing reverse sputtering to said layer insulation layer (11 -15) The process and (c) which process the front face of said layer insulation layer (11 -15) By carrying out sputtering of the metal which may improve the adhesion of a conductor pattern (C2 - C6), and carrying out sputtering of the copper if needed. The process which forms the substrate layer (UL) which consists of one sort or two sorts of metals on the processing side (TS) of said layer insulation layer (11 -15).

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a multilayer-interconnection plate and its manufacture approach.

[0002]

[Description of the Prior Art] When realizing a large-scale and high-speed computer system etc., small IC chip of high accumulation etc. is usually used, and it becomes an important technical problem to make it into the structure suitable for improvement in the speed, and to mount in a patchboard. For this reason, in recent years, improvement in the speed and the cures against densification, such as multilayering, and thinning, thin-film-izing of a conductor pattern (the so-called finization), are demanded also about the patchboard for carrying IC chip etc.

[0003] As an approach of forming a metal conductor pattern in a patchboard, the subtractive process which uses copper clad laminate as a start ingredient is widely known from before. Moreover, recently, the additive process which forms a conductor pattern only with nonelectrolytic plating attracts attention as an option which changes to a subtractive process. Here, the manufacture procedure of the common multilayer-interconnection plate by the additive process (fully-additive process) is described briefly.

[0004] First, the adhesives for additives for forming a layer insulation layer are applied to the substrate front face which has a inner layer conductor pattern by the roll coater etc. These adhesives make a resin matrix distribute a meltable filler to a roughening agent. After said adhesives pass through exposure development and hardening processing, they are roughened by roughening agents, such as a chromic acid. Consequently, the filler in an adhesives layer is dissolved partially and a roughening side is formed in the front face of an adhesives layer. A catalyst nucleus required for the deposit of the beginning of plating is given to the roughening side of an adhesives layer, and plating resist is further formed of exposure development. Then, a conductor pattern is formed by performing non-electrolytic copper plating to a resist agensis part.

[0005] By repeating the procedure of the above conductor pattern formation if needed, the so-called build up multilayer-interconnection plate with which laminating formation of a layer insulation layer and the conductor pattern was carried out by turns on the substrate can be obtained.

[0006]

[Problem(s) to be Solved by the Invention] However, in the conventional full additive process, since the adhesives spreading, roughening, catalyst nucleus grant, and radio solution copper plating process of having mentioned above is required, the whole activity is complicated. However, the predetermined adhesion force is secured between layer insulation layers, and in order to obtain the conductor pattern which cannot exfoliate easily, there is a situation that neither of the above-mentioned processes can be skipped.

[0007] Moreover, in the full additive process, the roll coater is used as a general means to apply adhesives to a substrate front face. A roll coater has an parallel slot and is conventionally known as a coater which consists of a doctor bar arranged by approaching the roll of the pair arranged

by separating a predetermined gap, and an upper roll.

[0008] However, even if it is going to apply adhesives thinly using such equipment, thickness control becomes difficult and the problem that a smooth and uniform layer insulation layer cannot be obtained arises. In this case, by roughening of a layer insulation layer, irregularity becomes easy to be made on a front face, and the formation precision of a conductor pattern, the electrical property of a patchboard, etc. will get worse as a result.

[0009] Furthermore, the chemicals used at a roughening process have many harmful things to the body like a chromic acid or potassium permanganate generally. Therefore, the manufacturer of a patchboard needs to plan a certain antipollution measure like discarding chemicals carefully etc. However, when such a cure is performed, there is a problem of becoming cost quantity inevitably.

[0010] This invention is made in view of the above-mentioned situation, and the 1st purpose is in offering the multilayer-interconnection plate which can obtain the conductor pattern which cannot exfoliate easily, without roughening the layer insulation layer by chemicals.

[0011] The 2nd purpose of this invention is to offer the manufacture approach of the multilayer-interconnection plate which can raise the smooth nature of a layer insulation layer, and homogeneity since the thickness control of a layer insulation layer is easy, and can raise adhesion, formation precision, etc. of a conductor pattern certainly.

[0012] The 3rd purpose of this invention can simplify a production process, and is to offer the manufacture approach of the multilayer-interconnection plate which can moreover reduce a manufacturing cost.

[0013]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, in invention according to claim 1 In the multilayer-interconnection plate which comes to carry out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern on a substrate by turns The multilayer-interconnection plate equipped with the conductor pattern constituted by the metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern, and the copper-plating layer formed on said metal thin layer is made into the summary.

[0014] In the multilayer-interconnection plate which comes to carry out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern on a substrate in invention according to claim 2 by turns The metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern. The multilayer-interconnection plate equipped with the conductor pattern constituted by the copper thin layer formed by carrying out sputtering of the copper on said metal thin layer and the copper-plating layer formed on said copper thin layer is made into the summary.

[0015] In the manufacture approach of the multilayer-interconnection plate which carries out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern by turns on a substrate in invention according to claim 3 it is following (a) at least. - (e) Process, i.e., (a), By carrying out the spin coat of the resin on a substrate The process and (b) which form a layer insulation layer By performing reverse sputtering to said layer insulation layer The process and (c) which process the front face of said layer insulation layer By carrying out sputtering of the metal which may improve the adhesion of a conductor pattern, and carrying out sputtering of the copper if needed The process and (d) which form the substrate layer which consists of one sort or two sorts of metals on the processing side of said layer insulation layer By giving copper plating, where plating resist is formed on said substrate layer The process and (e) which form a copper-plating layer in the predetermined part on said substrate layer By etching the substrate layer located said plating resist and under the plating resist The manufacture approach of the multilayer-interconnection plate characterized by performing the process which forms the conductor pattern constituted by a substrate layer and the copper-plating layer one by one is made into the summary.

[0016] In the manufacture approach of the multilayer-interconnection plate which carries out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern by turns on a substrate in invention according to claim 4 it is following (a) at least. - (f) Process,

i.e., (a), By carrying out the spin coat of the resin on a substrate The process and (b) which form a layer insulation layer By performing reverse sputtering to said layer insulation layer. The process and (c) which process the front face of said layer insulation layer By carrying out sputtering of the metal which may improve the adhesion of a conductor pattern, and carrying out sputtering of the copper if needed. The process and (d) which form the substrate layer which consists of one sort or two sorts of metals on the processing side of said layer insulation layer. By etching, where a resist is formed on said substrate layer. The process and (e) which make the substrate layer the shape of a predetermined pattern. The process and (f) which exfoliate said resist from the substrate layer etched in the shape of a pattern By performing non-electrolytic copper plating or electrolytic copper plating to said substrate layer. The manufacture approach of the multilayer-interconnection plate characterized by performing the process which forms the conductor pattern constituted by a substrate layer and the copper-plating layer one by one is made into the summary.

[0017]

[Function] Since the metal which may improve the adhesion of a conductor pattern as a metal for metal thin film formation is used according to the multilayer-interconnection plate of this invention, the conductor pattern which cannot exfoliate easily can be obtained. Moreover, in this invention, being formed by the physical forming-membranes method of sputtering characterizes a metal thin layer. And generally the metal thin layer by sputtering is precise and smooth, and becoming the thing excellent in adhesion force is known. Therefore, even if it does not roughen the layer insulation layer by chemicals according to this invention from which such a metal thin layer serves as a substrate of a copper-plating layer, it becomes possible to raise the adhesion of a conductor pattern.

[0018] And since [ according to the manufacture approach of the multilayer-interconnection plate of this invention ] resin is applied with a spin coat, even when it is going to obtain the layer insulation layer of closing in, thickness control can be performed easily. Therefore, the smooth nature of a layer insulation layer and homogeneity can be raised, and adhesion, formation precision, etc. of a conductor pattern can be certainly raised as the result. Since the front face of a layer insulation layer will be processed by reverse sputtering, it becomes unnecessary moreover, to perform roughening by chemicals in advance of formation of a conductor pattern according to this manufacture approach. Therefore, a production process is simplified and, moreover, a manufacturing cost is reduced.

[0019] Hereafter, the manufacture approach is explained to a detail for the multilayer-interconnection plate of this invention in order of a process. In this invention, the substrate made of the product made from a ceramic sintered compact, metal, and a plastic can be used as a substrate for carrying out laminating formation of a layer insulation layer and the conductor pattern by turns.

[0020] As a substrate made from a ceramic sintered compact, there are an aluminum nitride (AlN) substrate, an alumina (aluminum 2O3) substrate, a boron nitride (BN) substrate, a silicon nitride (Si3N4) substrate, a mullite (3aluminum2 O3 and 2SiO2) substrate, etc., for example. As a metal substrate, there are a phosphor bronze substrate, an aluminum (aluminum) substrate, an alumite substrate, an iron (Fe) substrate, a copper (Cu) substrate, etc., for example. When producing the multilayer-interconnection plate which thought heat dissipation nature etc. as important, it is good to choose the substrate made from a ceramic sintered compact, and it good to choose an aluminum nitride substrate especially with high thermal conductivity especially. Moreover, when producing the multilayer-interconnection plate which thought low cost nature, workability, etc. as important, it is desirable to choose the substrate made of metal or a plastic. [0021] The conductor pattern of the 1st layer which consists of one sort or two or more sorts of metals by the conventionally well-known forming-membranes method of sputtering etc. if needed is formed in the front face of said substrate. In order to form a layer [ 1st ] layer insulation layer on the substrate with which the conductor pattern was formed, the spin coat of the resin of photosensitive or nonphotosensitivity is carried out. A spin coat method is the method of application which is made to rotate a substrate where a fluid is supplied on the substrate laid horizontally, and spreads a fluid over homogeneity thinly according to a centrifugal force at the

whole substrate. And in enforcing such a spin coat method, the coater called a spin coater is usually used.

[0022] As resin for layer insulation layers, there are polyimide resin, polyamide resin, an epoxy resin, BT (bismaleimide triazine) resin, BCB (divinyl siloxane screw benz-cyclo-butene) resin, polyester resin, conversion polyimide resin, conversion BT resin, a conversion epoxy resin, triazine resin, a polybutadiene resin, Pori Sall John resin, polyether aphen resin, polyetherimide resin, polyphenylene oxide resin, phenol resin, a urea resin, etc., for example. [0023] It is desirable to choose a comparatively cheap thing like an epoxy resin or BT resin especially as resin to be used. The reason is advantageous [ using these resin / like ], when attaining low cost-ization of a multilayer-interconnection plate. Moreover, it is desirable to choose what has the amount of hardening contraction small in choosing what has low reactivity with copper as resin to be used. As resin which fulfills the above-mentioned conditions, there are an epoxy resin, BT resin, etc., for example.

[0024] In addition, it is desirable to give photosensitivity to the resin for layer insulation stratification enumerated previously. The reason is photolithographies, such as exposure and development, can be performed and possible [ raising the formation precision of a layer insulation layer more ], if it is resin which gave photosensitivity. Moreover, the hole for forming the interstitial via hole (it only abbreviating to IVH hereafter) which aims at the electric flow between each class is formed in a layer insulation layer if needed.

[0025] As for the thickness of the resin applied by the spin coater, it is good that it is 5 micrometers - about 70 micrometers, and, as for the thickness of the layer insulation layer finally obtained, it is good that it is 3 micrometers - about 50 micrometers. The case where it becomes impossible to cover a conductor pattern with resin completely as the thickness of the resin applied is less than 5 micrometers may arise. When this thickness exceeds 50 micrometers, it becomes impossible on the other hand, to employ the advantage of a spin coat method efficiently. Moreover, it is because it is desirable when attaining lamination of the whole patchboard, holding a suitable electrical property to make thickness of a layer insulation layer into said within the limits.

[0026] Next, the procedure which forms the conductor pattern and layer insulation layer after the 2nd layer is explained. In advance of metal sputtering, reverse sputtering is performed in a layer [ 1st ] layer insulation layer. Reverse sputtering points out the thing of sputtering performed by making a target material side in cathode the bottom of an inert gas ambient atmosphere, and making reverse the aforementioned cathode and anode plate unlike the usual sputtering which makes a substrate side an anode plate and performs it. That is, when reverse sputtering is carried out, the ion of inert gas can draw near to a substrate side, and the front face of a substrate will be processed by the impact at that time. And so to speak, "it will be roughened physically" by the front face of a layer insulation layer by passing through such reverse sputtering. The advantage of processing by such reverse sputtering is being able to perform metal sputtering immediately within the equipment same after processing.

[0027] As inert gas filled in a high vacuum tub at the time of reverse sputtering, there are nitrogen, an argon, helium, neon, a krypton, etc., for example. When inert gas is used as an argon, there is an advantage that the adhesion of the metal thin layer formed of sputtering becomes good. Moreover, when inert gas is used as nitrogen, the residue when etching a metal thin layer stops being able to remain easily, and there is an advantage that the insulation between conductor patterns becomes good.

[0028] On the processing side of the layer [ 1st ] layer insulation layer by which surface treatment was carried out, a metal thin layer is formed of metal sputtering which may improve the adhesion of a conductor pattern. And on this metal thin layer, a copper thin layer is formed of copper sputtering. Consequently, it will be in the condition that the substrate layer which consists of one sort or two sorts of metals was prepared on the processing side of a layer insulation layer.

[0029] The metal which may improve the adhesion of a conductor pattern here points out chromium, nickel, titanium, iron, a tungsten, molybdenum, aluminum, cobalt, etc. The metal thin layer obtained by sputtering of these metals is precise and smooth, and it is because it becomes

the thing excellent in the adhesion force to a layer insulation layer. Moreover, it is because the above-mentioned metal thin layer is easily removable with the etchant of the simple presentation which does not contain an oxidizing agent, so it is convenient to pattern formation. In the adhesion of copper plating to a metal thin layer, said copper thin layer is formed if needed, in order to raise the adhesion between height, a copper-plating layer, and a metal thin layer. [0030] In this case, it is desirable to set thickness of a metal thin layer to 0.05 micrometers - about 0.3 micrometers, and to set thickness of a copper thin layer to 0.05 micrometers - about 0.6 micrometers. Moreover, as for the thickness in the total of a substrate layer, it is good that it is about 1.0 micrometers or less.

[0031] Dispersion arises that the thickness of a metal thin film is below said range in adhesion with a layer insulation layer, and it becomes easy to produce un-arranging, such as exfoliation and bulging. On the other hand, although time amount and cost start sputtering as the thickness of a metal thin layer is above said range, there is no great difference in the effectiveness acquired. There is a possibility that it may become impossible to fully improve the adhesion of a copper-plating layer as the thickness of a copper thin layer is below said range. On the other hand, although time amount and cost start sputtering as the thickness of a copper thin layer is above said range, there is no great difference in the effectiveness acquired.

[0032] In addition, when nickel is chosen as a metal which carries out sputtering, it is also possible to omit sputtering of the copper to a metal thin layer top. The reason of the adhesion of copper plating to nickel is comparatively good, and is because it may be necessary to necessarily form a copper thin layer.

[0033] Predetermined plating resist is formed on a substrate layer, and electrolytic copper plating or non-electrolytic copper plating is performed in this condition. Consequently, a copper-plating layer is formed in the front face of a substrate layer.

[0034] Since it is the metal layer which functions as a substantial conductor layer for making it flow through the electrical and electric equipment, said copper-plating layer is formed a little more thickly compared with a substrate layer. However, when a copper-plating layer becomes thick too much, a surface level difference becomes large and a possibility of causing trouble is in spreading of the resin by the spin coater. When an example is taken in this situation, it is good to set up the thickness of a copper-plating layer within the limits of 2 micrometers - 10 micrometers more preferably within the limits of 2 micrometers - 30 micrometers.

[0035] After forming a copper-plating layer, the substrate layer located plating resist which became unnecessary, and under the plating resist is removed by etching. The conductor pattern of the 1st layer constituted by the substrate layer which consists of one sort or two sorts of metals by this processing, and the copper-plating layer is obtained.

[0036] In this case, in order to attain shortening and process simplification of production time, it is desirable like copper, nickel and copper, chromium and copper, and titanium to use the etchant which can dissolve two or more sorts of metals in coincidence. As an example of the above etchant, the mixed water solution of the fluorine acid and the nitric acid which may dissolve copper and nickel in coincidence is mentioned.

[0037] Moreover, where a resist is formed beforehand, after etching a substrate layer in the shape of a pattern as an approach of forming the conductor pattern of the 1st layer, it is also possible to take the approach of exfoliating the resist and forming a copper-plating layer. And on the substrate in which the conductor pattern was formed by one of approaches, a layer [ 2nd ] layer insulation layer is formed by carrying out the spin coat of the resin again. And the above processes (formation of the substrate layer by the spin coat of resin and sputtering and formation of a copper-plating layer) are performed repeatedly if needed.

[0038]

[Working Example(s) and Comparative Example(s)] Hereafter, the examples 1-11 which materialized this invention, and the example of a comparison of those are explained to a detail based on a drawing.

[Example 1]

process (1): — as a substrate — the phosphor bronze substrate (Cu-Sn=95:4.8:0.2) 1 — choosing — conductor pattern C1 of the 1st layer on this phosphor bronze substrate 1 melanism

— it processed

[0039] Process (2): The photosensitive epoxy resin which consists of the following presentation as resin for layer insulation stratification was prepared.

Cresol novolak acrylate resin: 66 % of the weight, bisphenol A mold resin: 21 % of the weight  
Sensitizer: 6 % of the weight, curing agent: 3 % of the weight, Photopolymerization agent: 3 % of the weight  
Interface regulator: As shown in 1 % of the weight, and drawing 1 (a), this resin was applied on the phosphor bronze substrate 1 using the spin coater (the Mikasa, Inc make, trade name: I-H-DX). In addition, layer insulation layer I1 finally obtained in this example, the thickness of the resin to apply was set as 30 micrometers so that thickness might be set to 20 micrometers.

[0040] Process (3): After prebaking a photosensitive epoxy resin, exposure and development were performed and 180 degrees C and cure processing for 60 minutes were further performed to the photosensitive epoxy resin. Layer [ 1st ] layer insulation layer I1 equipped with the hole 2 with a diameter of about 30 micrometers for IVH formation by the above processing as shown in drawing 1 (b) It obtained.

[0041] Process (4): Next use a vacuum sputtering system (made in the Tokuda factory, CFS-8EP), and it is the layer insulation layer I1 in nitrogen-gas-atmosphere mind. Receiving time sputtering was performed. At that time, gas pressure was set to 0.8Pa and sputtering time amount was set as for 2 minutes. By this reverse sputtering, it is the layer insulation layer I1. It is the processing side TS upwards, it formed.

[0042] Process (5): It is the layer insulation layer I1 by subsequently carrying out sputtering of the chromium using the same vacuum sputtering system. Processing side TS it is the chromium thin layer L1 with a thickness [ as a metal thin layer ] of 0.1 micrometers upwards. It formed. Furthermore, it is the chromium thin layer L1 by carrying out sputtering of the copper using the same vacuum sputtering system. It is the 0.2-micrometer copper thin layer L2 upwards. It formed. Consequently, as shown in drawing 1 (c), the substrate layer UL with a thickness of 0.3 micrometers it is thin from chromium and two sorts of copper metals was obtained.

[0043] In addition, in this example, by sputtering of chromium, gas pressure was set to 0.8Pa and sputtering time amount was made into 10 minutes. Moreover, in copper sputtering, gas pressure was set to 0.8Pa and sputtering time amount was made into 20 minutes.

[0044] The photopolymer for plating-resist formation (Tokyo adaptation make, OMR- 83/80cps) was applied on the substrate layer UL using process (6); next a spin coater. In addition, it set up so that the thickness of the plating resist 3 finally obtained might be set to 1 micrometer. And prebaking, exposure and development, and postbake were performed.

[0045] Consequently, as shown in drawing 1 (d), it is a conductor pattern (last shipment=30micrometer / 50 micrometers) C2. The plating resist 3 of the shape of a channel for forming was formed on the substrate layer UL

[0046] By carrying out electrolytic copper plating using process (7); next the following electrolytic copper plating bath, as shown in drawing 1 (e), it is the electrolytic copper plating layer L3 with a thickness of 10 micrometers on the substrate layer UL. It formed.

[0047] H2 SO4 and 5H2 O: 210 g/l H2 SO4 : 60 g/l, chlorine ion: 25 mg/l Additive: Small quantity  
Bath temperature: 28 degrees C and cathodic current consistency: 2.5 A/dm2 Processing time: 10 minutes

The plating resist 3 which became unnecessary was exfoliated from the substrate layer UL by etching with process (8); next the exfoliation liquid (Tokyo adaptation make, OMR exfoliation liquid) of dedication of the phosphor bronze substrate 1. Furthermore, copper thin layer L2 first located under plating resist 3 by using a nitric-acid water solution as etchant 10% it etched. Then, chromium thin layer L1 similarly located under plating resist 3 by using a hydrochloric-acid water solution as etchant 20% it etched. consequently, it is shown in drawing 1 (f) — as — chromium thin layer L1 Copper thin layer L2 from — the becoming substrate layer UL and the electrolytic copper plating layer L3 Conductor pattern C2 constituted it obtained.

[0048] Process (9): By carrying out by repeating a process (8) from said process (2), they are the conductor pattern C3 after the 3rd layer - C6. Layer insulation layer I2 -I5 after the 2nd layer Sequential formation was carried out. And the multilayer-interconnection plate 6 which has



a build up layer as finally shown in drawing 2 was obtained.

[0049] The multilayer-interconnection plate 6 obtained according to a series of above-mentioned processes is used, and they are the \*\* conductor pattern C2 - C6. The dimensional accuracy of the width of face of Rhine L, and \*\* layer insulation layer I1 - I5. The dimensional accuracy and the \*\* conductor pattern C2 of thickness - C6 Pull reinforcement was investigated. Those results are shown in Table 1.

[0050] A conductor pattern C2 - C6 When surveyed, it turned out that the width of face of Rhine L takes the value extremely approximated to 30 micrometers which is the set point. It turned out that the value which similarly was extremely approximated to 20 micrometers which is the set point also about the thickness of layer insulation layer I1 - I5 is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm<sup>2</sup> was acquired.

[Examples 2 and 3]

A process (1) - a process (4): It was based on the process (1) of an example 1 - the process (4).

[0051] Process (5): By carrying out sputtering of the titanium using the vacuum sputtering system mentioned above, it is the layer insulation layer I1. Processing side TS It is the titanium thin layer L1 with a thickness [as a metal thin layer] of 0.1 micrometers upwards. It formed. Furthermore, it is the titanium thin layer L1 by carrying out sputtering of the copper using the same vacuum sputtering system. It is the 0.2-micrometer copper thin layer L2 upwards. It formed. Consequently, as shown in drawing 1 (c), the substrate layer UL with a thickness of 0.3 micrometers it is thin from titanium and two sorts of copper metals was obtained.

[0052] A process (6) - a process (9): Based on the process (6) of an example 1 - the process (9), the multilayer-interconnection plate 6 as finally shown in drawing 2 was obtained after that. The result which the \*\*\* investigated using this multilayer-interconnection plate 6 is shown in Table 1. Consequently, a conductor pattern C2 - C6 The Rhine width of face is also layer insulation layer I1 - I5. It turned out that the value which approximated thickness as well as an example 1 to the set point extremely is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm<sup>2</sup> was acquired.

[0053] And as shown in Table 1, it is the metal thin layer L1. The suitable result was obtained about the example 3 which replaced the formation ingredient with nickel from titanium as well as examples 1 and 2. Moreover, it is the copper thin layer L2 only by one sort of etchant called fluoric acid/nitric-acid =1:3 water solution the case of an example 3. Nickel thin layer L1 There was an advantage that it could etch into coincidence.

[Examples 4-6]

Process (1): In the example 4, the alumina substrate (aluminum2 O3 =92%) 4 was chosen as a substrate. And it is the conductor pattern C1 of the 1st layer by carrying out sputtering of titanium, molybdenum, and the nickel on the alumina substrate 4. It formed.

[0054] Process (2): By applying the resin used in the example 1 using a spin coater, it is the conductor pattern C1 of the 1st layer. It is the layer insulation layer I1 upwards. It formed. In addition, layer insulation layer I1 finally obtained in this example 4 The thickness of the resin to apply was set as 17 micrometers so that thickness might be set to 10 micrometers.

[0055] A process (3) - a process (5): It was based on the process (3) of an example 1 - the process (5).

The photopolymer for plating-resist formation used in the example 1 on the substrate layer UL using process (6); next a spin coater was applied, and prebaking, exposure and development, and postbake were performed. Consequently, as shown in drawing 1 (d), it is a conductor pattern (last shipment=15micrometer / 20 micrometers) C2. The plating resist 3 of the shape of a channel for forming was formed on the substrate layer UL.

[0056] By carrying out electrolytic copper plating using process (7); next the electrolytic copper plating bath used in the example 1, as shown in drawing 1 (e), it is the electrolytic copper plating layer L3 with a thickness of 6 micrometers on the substrate layer UL. It formed.

[0057] A process (8) - a process (9): Based on the process (8) of an example 1 - the process (9), the multilayer-interconnection plate 6 as finally shown in drawing 2 was obtained after that. The result which the \*\*\* investigated using this multilayer-interconnection plate 6 is shown in

Table 1. Consequently, a conductor pattern C2 - C6 The Rhine width of face is also layer insulation layer I1 - I5. It turned out that the value which approximated thickness as well as an example 1 to the set point extremely is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm<sup>2</sup> was acquired.

[0058] And as shown in Table 1, it is the metal thin layer L1. The suitable result was obtained about the example 5 which replaced the formation ingredient with titanium from chromium, and the example 6 replaced with nickel from chromium as well as an example 4. Moreover, it is the copper thin layer L2 only by one sort of etchant called fluoric acid/nitric-acid =1:3 water solution the case of an example 6. Nickel thin layer L1 There was an advantage that it could etch into coincidence.

[Examples 7-9]

Process (1): In the example 7, the aluminum nitride substrate (AlN:Y2O3 =96:4) 1 was chosen as a substrate. And it is the conductor pattern C1 of the 1st layer by carrying out sputtering of titanium, molybdenum, and the nickel on the aluminum nitride substrate 1. It formed.

[0059] Process (2): By applying the resin used in the example 1 using a spin coater, it is the conductor pattern C1 of the 1st layer. It is the layer insulation layer I1 upwards. It formed. In addition, layer insulation layer I1 finally obtained in this example 7 The thickness of the resin to apply was set as 10 micrometers so that thickness might be set to 5 micrometers.

[0060] A process (3) - a process (5): It was based on the process (3) of an example 1 - the process (5).

The photopolymer for plating-resist formation used in the example 1 on the substrate layer UL using process (6); next a spin coater was applied, and prebaking, exposure and development, and postbake were performed. Consequently, as shown in drawing 1 (d), it is a conductor pattern (last shipment=4micrometer / 6 micrometers) C2. The plating resist 3 of the shape of a channel for forming was formed on the substrate layer UL.

[0061] By carrying out electrolytic copper plating using process (7); next the electrolytic copper plating bath used in the example 1, as shown in drawing 1 (e), it is the electrolytic copper plating layer L3 with a thickness of 1.5 micrometers on the substrate layer UL. It formed.

[0062] A process (8) - a process (9): Based on the process (8) of an example 1 - the process (9), the multilayer-interconnection plate 6 as finally shown in drawing 2 was obtained after that. The result which the \*\*\* investigated using this multilayer-interconnection plate 6 is shown in Table 1.

[0063] Consequently, in spite of very FAIN as compared with examples 1 and 2, they are a conductor pattern C2 - C6. The Rhine width of face is also layer insulation layer I1 - I5. It turned out that the value which also approximated thickness to the set point extremely is taken.

Subsequently, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm<sup>2</sup> was acquired.

[0064] And as shown in Table 1, it is the metal thin layer L1. The very suitable result was obtained about the example 8 which replaced the formation ingredient with titanium from chromium, and the example 9 replaced with nickel from chromium as well as an example 7.

Moreover, it is the copper thin layer L2 only by one sort of etchant called fluoric acid/nitric-acid =1:3 water solution the case of an example 9. Nickel thin layer L1 There was an advantage that it could etch into coincidence.

[Example 10]

A process (1) - a process (4): It was based on the process (1) of an example 1 - the process (4).

[0065] Process (5): By carrying out sputtering of the nickel using a vacuum sputtering system, it is the layer insulation layer I1. Processing side TS The nickel thin layer L1 (= the substrate layer UL which consists only of one sort of metals) with a thickness of 0.1 micrometers was formed upwards. In addition, about the gas pressure and time amount at the time of sputtering, it applied to the conditions of an example 1 correspondingly.

[0066] A process (6) - a process (7): It was based on the process (6) of an example 1 - the process (7).

Process (8): Plating resist 3 was first exfoliated from the substrate layer UL by etching with the

exfoliation liquid of dedication of the phosphor bronze substrate 1. Next, the nickel thin layer L1 located under plating resist 3 20%, using a hydrochloric-acid water solution as etchant was etched. Consequently, nickel thin layer L1 And electrolytic copper plating layer L3 Conductor pattern C2 constituted it obtained.

[0087] Process (9): By carrying out by repeating a process (2) - a process (8), they are the conductor pattern C3 after the 3rd layer - C8. Layer insulation layer 12 -15 after the 2nd layer Sequential formation was carried out. And the multilayer-interconnection plate 7 as finally shown in drawing 3 was obtained.

[0088] The result which the \*\*\*\* investigated using this multilayer-interconnection plate 7 is shown in Table 1. Consequently, a conductor pattern C2 - C8 The Rhine width of face is also layer insulation layer 11 -15. It turned out that the value which approximated extremely thickness as well as the multilayer-interconnection plate 6 of example 1 grade to the set point is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm2 was acquired.

[0089] That is, although only one sort of metals constitute the substrate layer UL from this example 10 thinly, it will be said that the engine performance comparable as examples 1-9 is obtained. And when such a configuration is adopted, the time amount of sputtering etc. decreases and it becomes in process, in cost, and advantageous.

[Example 11]

A process (1) - a process (5): Based on the process (1) of an example 2 - a process (5), as shown in drawing 4 (a) - drawing 4 (c), it is the layer insulation layer 11. The substrate layer UL was formed upwards.

[0070] The photopolymer for resist formation (the Hoechst A.G. make, trade name: AZ-4200) was applied on the substrate layer UL using process (6); next a spin coater. In addition, in this example, it set up so that the thickness of the resist 5 finally obtained might be set to 3 micrometers.

[0071] And as prebaking, exposure and development, and postbake are performed and it is shown in drawing 4 (d), it is a conductor pattern (last shipment=15micrometer / 20 micrometers) C2. The resist 5 of the shape of a channel for forming was formed on the substrate layer UL.

[0072] Copper thin layer L2 located under said resist 5 process (7); next by using a nitric-acid water solution as etchant 10% it etched. Then, chromium thin layer L1 similarly located under the resist 5 by using a hydrochloric-acid water solution as etchant 20% it etched. Consequently, as shown in drawing 4 (e), the substrate layer UL was made into the shape of a predetermined pattern.

[0073] Non-electrolytic copper plating was carried out using process (8); next the following non-electrolytic copper plating bath. It is the non-electrolytic copper plating layer L3 with a thickness of 6 micrometers on the substrate layer UL etched in the shape of a pattern by this non-electrolytic copper plating as shown in drawing 4 (f). It formed.

[0074] CuSO4 and 5H2 O:0.05 mol/l, HCHO: 0.12 mol/l and NaOH:0.15 mol/l EDTA and 4NaO.10 mol/l, KNI3 (CN) : 10 mg/l Alpha-alpha'-DIPICURURU: Small quantity, pH=12.5 Bath temperature : [ 60 degrees C. ] processing-time: - 2 hour -, consequently chromium thin layer L1 Copper thin layer L2 from - the becoming substrate layer UL and the non-electrolytic copper plating layer L3 Conductor pattern C2 constituted it obtained.

[0075] Process (9): By carrying out by repeating said process (2) - a process (8), they are the conductor pattern C3 after the 3rd layer - C8. Layer insulation layer 12 -15 after the 2nd layer Sequential formation was carried out. And the multilayer-interconnection plate 6 which has a build up layer as finally shown in drawing 2 was obtained.

[0076] The result which the \*\*\*\* investigated using this multilayer-interconnection plate 6 is shown in Table 1. Consequently, a conductor pattern C2 - C8 The Rhine width of face is also layer insulation layer 11 -15. It turned out that the value which approximated extremely thickness as well as the multilayer-interconnection plate 6 of example 1 grade to the set point is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm2 was acquired.

[The example of a comparison]

process (1): - the melanism after choosing copper clad laminate (FR-4) as a substrate and forming the inner layer conductor pattern of the 1st layer according to a well-known approach conventionally - it processed.

[0077] Process (2): The photosensitive epoxy resin which consists of the following presentation as resin for layer insulation stratification was prepared, and this resin was applied on the substrate using the roll coater.

Cresol novolak acrylate resin: 53 % of the weight, bisphenol A mold resin:17 % of the weight, epoxy resin filler:19 % of the weight Sensitizer: 5 % of the weight, curing agent:2 % of the weight Photopolymerization agent: 3 % of the weight Interface regulator: The thickness of the resin to apply was set as 90 micrometers so that the thickness of the layer insulation layer which is 1 % of the weight, and which is finally obtained might be set to 55 micrometers.

Process (3): After prebaking said resin, the layer [ 1st ] layer insulation layer was formed by [ for exposure, development and 150 degrees C. and 180 minutes ] carrying out cure processing. [0078] Process (4): After roughening the front face of a layer insulation layer by processing chrome oxide (CrO3) for about 60 minutes, the Pd-Sn catalyst nucleus was given to the roughening side. Subsequently, the photosensitive epoxy resin was applied to the thickness of 30 micrometers by the roll coater. And plating resist of the shape of a channel for forming a conductor pattern (last shipment=75micrometer / 75 micrometers) was obtained by drying this resin, and exposing and developing negatives.

[0079] Process (5): P After activating a d-Sn catalyst nucleus, non-electrolytic copper plating was carried out using the non-electrolytic copper plating bath for thickness attachment of the following presentation. With this non-electrolytic copper plating, the non-electrolytic copper plating layer with a thickness of 30 micrometers was formed in the plating-resist agensis part. [0080] CuSO4 and 5H2 O:0.05 mol/l HCHO:0.12 mol/l and NaOH:0.15 mol/l EDTA and 4NaO.10 mol/l, KNI3 (CN) : 10 mg/l Alpha-alpha'-DIPICURURU: Small quantity, pH=12.5 Bath temperature: 60 degrees C Processing time: 6 hours

Process (6): By carrying out by repeating said process (2) - a process (5), sequential formation of the conductor pattern after the 3rd layer and the layer insulation layer after the 2nd layer was carried out. And the additive multilayer-interconnection plate which finally has a build up layer was obtained.

[0081] The result which the \*\*\*\* investigated using the multilayer-interconnection plate of the example of a comparison is shown in Table 1. Consequently, the result that the dimension error of the Rhine width of face of a conductor pattern became large compared with the time of examples 1-11 was obtained. Moreover, the result with the same said of the dimension error of the thickness of a layer insulation layer was obtained. That is, in the case of the multilayer-interconnection plate of the example of a comparison, it was expected with the irregularity of the front face resulting from aggravation and roughening of the smooth nature of a layer insulation layer etc. that aggravation of the formation precision of a conductor pattern, the electrical property of a patchboard, etc. was brought about. Furthermore, when pull reinforcement was measured, it stopped at the low value of 1.0 kgf/mm2 which are a value below abbreviation one half of examples 1-11.

[0082] Moreover, when the manufacture approach of the example of a comparison was compared with the manufacture approach of examples 1-11, it was checked that production time becomes [ the way of the former which needs a roughening process and a thickness attachment radio solution copper-plating process ] long generally.

[0083]

[Table 1]

unnecessary. Therefore, a production process can be simplified and the outstanding effectiveness that a manufacturing cost can moreover be reduced is done so.

[Translation done.]

	基板	※1	導体パターン (μm)				絶縁層 (μm)
			L1	L2	L3 ※2	L/S	
実施例1	りん青銅	①	Cr 0.1	Cu 0.2	電Cu 10	30/50	20
実施例2	りん青銅	①	Ti 0.1	Cu 0.2	電Cu 10	30/50	20
実施例3	りん青銅	①	Ni 0.1	Cu 0.2	電Cu 10	30/50	20
実施例4	Al <sub>2</sub> O <sub>3</sub>	①	Cr 0.1	Cu 0.2	電Cu 6	15/20	10
実施例5	Al <sub>2</sub> O <sub>3</sub>	①	Ti 0.1	Cu 0.2	電Cu 6	15/20	10
実施例6	Al <sub>2</sub> O <sub>3</sub>	①	Ni 0.1	Cu 0.2	電Cu 6	15/20	10
実施例7	AIN	①	Cr 0.1	Cu 0.2	電Cu 1.5	4/8	5
実施例8	AIN	①	Ti 0.1	Cu 0.2	電Cu 1.5	4/8	5
実施例9	AIN	①	Ni 0.1	Cu 0.2	電Cu 1.5	4/8	5
実施例10	りん青銅	①	Cr 0.1	Cu 0.2	電Cu 10	30/50	20
実施例11	Al <sub>2</sub> O <sub>3</sub>	②	Cr 0.1	Cu 0.2	無電Cu 6	15/20	10
比較例	FR-4	-	-	-	無電Cu30	75/75	55

注: ※1...表中①は請求項3に記載の製造方法を示し、②は請求項4に記載の製造方法を示している。  
 ※2...「電Cu」は電解めっきを意味し、「無電Cu」は無電解めっきを意味している。

[0084]

[Table 2]

	導体パターンのLの幅		層間絶縁層の膜厚		プル強度	
	設定値	実測値	設定値	実測値	kgf/mm <sup>2</sup>	
実施例1	30	30.5±1.0	μm	20	20.0±2.5	μm
実施例2	30	28.6±1.5		20	20.2±3.1	
実施例3	30	30.7±1.4		20	20.3±2.7	
実施例4	15	14.5±1.5		10	10.0±3.0	
実施例5	15	15.4±1.2		10	9.8±2.5	
実施例6	15	15.3±1.3		10	10.4±2.6	
実施例7	4	4.3±1.1		5	5.2±1.9	
実施例8	4	3.7±0.8		5	5.1±2.0	
実施例9	4	4.1±0.9		5	4.9±1.7	
実施例10	30	30.2±1.5		20	19.8±2.8	
実施例11	15	15.2±1.3		10	10.2±2.7	
比較例	75	75.0±5.0		55	55.0±10.0	
						1.0

[0085] In addition, of course, modification within the limits which do not deviate from the meaning of invention, such as not being limited only to each above-mentioned example, for example, increasing or decreasing the number of layers of a build up layer, is possible for this invention.

[0086]

[Effect of the Invention] As explained in full detail above, with the multilayer-interconnection plate of this invention, the outstanding effectiveness that the conductor pattern which cannot exfoliate easily can be obtained is done so, without roughening the layer insulation layer by chemicals, since it is characterized by performing metal sputtering which may improve the adhesion of a conductor pattern.

[0087] Moreover, by the manufacture approach of the multilayer-interconnection plate of this invention, the approach of applying the resin for forming a layer insulation layer by the spin coater is adopted. For this reason, according to this manufacture approach, the thickness control of a layer insulation layer becomes easy, and the outstanding effectiveness that it can have, and the smooth nature of a layer insulation layer and homogeneity can be raised, and adhesion, formation precision, etc. of a conductor pattern can be raised certainly is done so. [0088] And similarly in order [ according to this manufacture approach ] to perform surface treatment of the layer insulation layer by reverse sputtering, roughening by chemicals becomes